1. A semiconductor device, comprising:

a semiconductor die; and

an electronic circuit located on said die; and

a via having a via top portion beginning at a top surface of said die and extending through said die to a via bottom portion on a bottom surface of said die;

an input/output (I/O) interconnect physically and electrically coupled to said via bottom portion, said I/O interconnect structure being located within an area on the bottom surface of said die; and

an I/O signal line coupled to said electronic circuit and said I/O interconnect structure by passing through said via;

wherein electrical signals can be communicated through said I/O signal line and said I/O interconnect structure between said electronic circuit and a second semiconductor device, which second semiconductor device is separate from the first semiconductor device.

2. The device of claim 1, further including a plurality of additional I/O interconnects, and wherein all of said I/O interconnects are located within a surface area corresponding to the bottom surface of said die.
3. The device of claim 2, further wherein said I/O interconnects occupy more than half of the bottom surface area of said die.
4. The device of claim 3, further wherein said electronic circuit occupies substantially all of said top surface area of said die.
5. The device of claim 1, wherein such die is formed such that no I/O interconnects are located on said top surface of said die.
6. The device of claim 1, wherein substantially all of said top surface of said die is used for said electronic circuit, and no I/O interconnects are located on said top surface of said die.

7. The device of claim 1, further including a plurality of additional I/O interconnects, and wherein a first portion of said plurality of I/O interconnects are located within a surface area corresponding to the bottom surface of said die, and a second portion of said plurality of I/O interconnects are located within a surface area corresponding to the top surface of said die.

8. The device of claim 1, wherein said electronic circuit and said I/O interconnects are integrated on opposite sides of a single die.

9. The device of claim 5, wherein said device is contained within a single semiconductor wafer including a plurality of additional identical devices, and wherein a top surface of said wafer includes only die for such devices.

10. The device of claim 1, wherein said vias are filled with conductive material.

11. The device of claim 10, wherein said top portion of said via is coupled to a top side conductive pad located on the top side of said die.

12. The device of claim 8, wherein said top portion and said bottom portion of said via are different in size.

13. The device of claim 1, wherein said I/O interconnect is a bottom side conductive pad located on the bottom side of said die.

14. The device of claim 13, wherein said top portion of said via is coupled to a top side conductive pad located on the top side of said die, and wherein said top side conductive pad is smaller than said bottom side conductive pad.

15. The device of claim 1, wherein said I/O interconnect includes a conductive bump structure.

16. A multi-chip electronic circuit, comprising:

a first and second semiconductor die; and

a first electronic circuit being located on said first die; and

a second electronic circuit being located on said second die; and

said first semiconductor die including a first via, which first via has a first via top portion beginning at a first top surface of said first die and extending through said first die to a first via bottom portion on a first bottom surface of said first die;

a first input/output (I/O) interconnect physically and electrically coupled to said first via bottom portion, said first I/O interconnect structure being located within a first area on the first bottom surface of said first die; and

a first I/O signal line coupled to said first electronic circuit and said first I/O interconnect structure by passing through said first via;

a second input/output (I/O) interconnect electrically coupled to said second electronic circuit, and further being physically and electrically coupled to said first I/O interconnect;

wherein electrical signals can be communicated between said first and second electronic circuits through said first and second I/O interconnects.

17. The circuit of claim 16, further wherein:

said first I/O interconnect includes a first conductive bump structure;

said second I/O interconnect includes a second conductive bump structure; and

further wherein said first and second conductive bumps are joined together to form an electronic signal path.

18. The circuit of claim 16, further wherein:

said first I/O interconnect includes a conductive bump;

said second I/O interconnect includes a bond pad; and

further wherein said conductive bump and bond pad are joined together to form an electronic signal path.

19. The circuit of claim 16, further wherein

said second semiconductor die includes a second via, which second via has a second via top portion beginning at a second top surface of said second die and extending through said second die to a second via bottom portion on a second bottom surface of said second die; and

said second input/output (I/O) interconnect is electrically coupled to said second via top portion.

20. The circuit of claim 19, further wherein said second semiconductor die includes a third I/O interconnect, which third I/O interconnect is located on said second bottom surface of said second die and is coupled to said second via bottom portion.

21. The circuit of claim 20, further including:

a third semiconductor die; and

a third electronic circuit being located on said third die; and

a fourth input/output (I/O) interconnect electrically coupled to said third electronic circuit, and further being physically and electrically coupled to said third I/O interconnect;

wherein electrical signals can be communicated between said second and third electronic circuits through said third and fourth I/O interconnects.

22. A chip scale package for a semiconductor device containing a plurality of electronic circuits, said chip scale package comprising:

a semiconductor body having a size and shape configured to accommodate the plurality of electronic circuits in the semiconductor device; and

a via having a via top portion starting at a top surface of said body and extending to a via bottom portion on a bottom surface of said body;

an input/output (I/O) interconnect physically and electrically coupled to said via bottom portion, said I/O interconnect structure being located within an area on the bottom surface of said die; and

an I/O signal line formed of a conductive material passing through said via and coupled to said said I/O interconnect structure;

wherein said packaging for the device is formed prior to the formation of any of the plurality of electronic circuits.

23. The package of claim 22, further including a plurality of additional I/O interconnects, and wherein all of said I/O interconnects are located within a surface area corresponding to the bottom surface of said body.

24. The package of claim 22 wherein said electronic circuit and said I/O interconnects can be formed on opposite sides of said semiconductor body.

25. The package of claim 22, wherein said package is contained within a single semiconductor wafer including a plurality of additional identical packages.

26. The package of claim 22, wherein said vias are filled with conductive material.

27. The package of claim 22, wherein said top portion of said via is coupled to a top side conductive pad located on the top side of said body.

28. The package of claim 22, wherein said I/O interconnect is a bottom side conductive pad located on the bottom side of said body.

29. The package of claim 28, wherein said top portion of said via is coupled to a top side conductive pad located on the top side of said die, and wherein said top side conductive pad is smaller than said bottom side conductive pad.

30. The package of claim 22, wherein said I/O interconnect includes a conductive bump structure.

31. A method of forming a chip scale package for a semiconductor device, comprising the steps of:

(a) providing a semiconductor body; and

(b) forming a via having a via top portion beginning at a top surface of said body and extending through said body to a via bottom portion on a bottom surface of said body; and

(c) forming an input/output (I/O) interconnect physically and electrically coupled to said via bottom portion, said I/O interconnect structure being located within an area on the bottom surface of said body; and

(d) forming an I/O signal line using conductive material via that is coupled to said I/O interconnect structure through said via;

wherein said package is formed prior to the formation of any electronic circuits located in said semiconductor body.

32. The method of claim 31, wherein said via is formed using mechanical drilling, laser drilling, or a dry etching process.

33. The method of claim 31, further including a step (c') prior to (c): forming electronic circuits in said semiconductor body as part of a die for the semiconductor device.

34. The method of claim 33, further including a step of forming a filler material in said via after step (b), which filler material is left in place until after said step (c').

35. The method of claim 31, wherein said (I/O) interconnect is bond pad and/or a conductive bump.

36. A method of forming a semiconductor device, comprising the steps of:

forming a semiconductor die; and

forming a via having a via top portion beginning at a top surface of said die and extending through said die to a via bottom portion on a bottom surface of said die;

forming an electronic circuit located on said die; and

forming an input/output (I/O) interconnect physically and electrically coupled to said via bottom portion, said I/O interconnect structure being located within an area on the bottom surface of said die; and

forming an I/O signal line coupled to said electronic circuit and said I/O interconnect structure by passing through said via;

wherein electrical signals can be communicated through said I/O signal line and said I/O interconnect structure between said electronic circuit and a second semiconductor device, which second semiconductor device is separate from the first semiconductor device.

37. The method of claim 36, wherein said via is formed after said electronic circuit.

38. The method of claim 37, wherein said via is formed using reactive ion etching.

39. The method of claim 36, further including a step of forming a filler material in said via, which filler material is left in place until after said electronic circuit is formed.

40. The method of claim 37, further including a step of forming a conductive layer in said via, which conductive layer forms part of said I/O signal line.

41. The method of claim 36, wherein said via top portion is smaller than said via bottom portion.

42. The method of claim 36, wherein said (I/O) interconnect is bond pad and/or a conductive bump.

43. A semiconductor device, comprising:

a semiconductor die, said die having a top surface, a bottom surface, and a plurality of side surfaces; and

an electronic circuit located on top surface of said die; and

a plurality of input/output (I/O) interconnects physically located on one or more of said plurality of side surfaces;

a plurality of I/O signal lines, each of said I/O signal lines being coupled to one or more of said plurality of said I/O interconnects;

wherein said I/O interconnects are configured so that they are capable of forming a frictional contact fit with corresponding mating interconnects coupled to a second electronic circuit which is not formed as part of said semiconductor die.

44. The device of claim 43, further including a semiconductor device mating receptacle, which mating receptacle includes a plurality of mating interconnects adapted to form a frictional contact with corresponding ones of said plurality of I/O interconnects.

45. The device of claim 44, wherein said mating receptacle includes a plurality of contact leads coupled to said plurality of mating interconnects for carrying signals from said electronic circuit to said second electronic circuit.

46. A method of forming a semiconductor device interconnect comprising the steps of:

providing a first semiconductor die, said die having a top surface, a bottom surface, and a plurality of side surfaces; and

providing an electronic circuit located on a top surface of said die; and

providing a plurality of input/output (I/O) interconnects physically located on one or more of said plurality of side surfaces;

providing a plurality of I/O signal lines, each of said I/O signal lines being coupled to one or more of said plurality of said I/O interconnects;

inserting said die into a mating receptacle adapted for said die, said mating receptacle including a plurality of mating interconnects adapted to form a frictional contact with corresponding ones of said plurality of I/O interconnects when said die is physically forced into said mating receptacle, so as to form a signal interconnect between said electronic circuit and a second electronic circuit which is not originally formed to be electrically connected to said semiconductor die; and

wherein said signal interconnect is formed without the use of soldering, or any additional temperature treatments, including reflow.

47. The method of claim 46, wherein said mating interconnects are comprised of particle enhanced interconnect material.

48. The method of claim 46, wherein said die is first combined with a chip scale package side before being inserted into said mating receptacle, and said chip scale package includes couples to said plurality of I/O interconnects and extends such interconnects to said mating interconnects.